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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,929	10/09/2003	Chul M. Jung	MICS:0115	7755

7590 03/06/2006

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EXAMINER	
SOFOCLEOUS, ALEXANDER	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/681,929	**Applicant(s)** JUNG, CHUL M.
	Examiner Alexander Sofocleous	**Art Unit** 2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.
 4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1,4-6,8-10 and 12-15* is/are rejected.
7)☒ Claim(s) *2,5,7,11* is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a)☐ All b)☐ Some * c)☐ None of:
  1.☐ Certified copies of the priority documents have been received.
  2.☐ Certified copies of the priority documents have been received in Application No. _____.
  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
4) ☑ Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *EAST Search History*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed October 9 2003.

2. Claims 1-20 are pending in the case. Claims 16-20 are withdrawn from consideration. Claims 1, 4, 6, 10, 16 and 18 are independent claims.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 1-15, drawn to a memory with equalizer circuitry, classified in class 365, subclass 203.

Group II. Claims 16-17, drawn to method for accessing the memory, classified in class 365, subclass 189.01.

Group III. Claims 18-20, drawn to method for producing the memory, classified in class 365, subclass 149.

Inventions Group II, III and Group I are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another and materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the processes can be used with other memory circuits.

Because these inventions are independent or distinct for the reasons given above and have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Attorney Michael Fletcher (Reg No. 32,777) on February 23, 2006 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-15. Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-20 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

4. The drawings are objected to because the long bitline (Fig. 5 [214]) should be labeled --316-- (see Page 8, line 21).

5. Figure 2 and Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 1, 3-4, 6, and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Busch et al. (U.S. Patent 4,807,195).**

Regarding independent claim 1, Busch et al. show an equalization circuit (Fig. 5) comprising:

a first sense amplifier (Fig. 5 [405]) having an input (Fig. 5 [450]), the input being electrically isolated from an input (Fig. 5 [440]) to a second sense amplifier (Fig. 5 [400]);

an equalizer (Fig. 5 [T7]) connected to the input (Fig. 5 [450]) to the first sense amplifier (Fig. 5 [405]) to provide an equalizing voltage to the input to the first sense amplifier;

and wherein the input (Fig. 5 [450]) to the first sense amplifier (Fig. 5 [405]) may be equalized by the equalizing voltage independent from the input (Fig. 5 [440]) to the second sense amplifier (Fig. 5 [400]).

Regarding dependent claim 3, Busch et al. show the input (Fig. 5 [450]) to the first sense amplifier (Fig. 5 [405]) comprises a bitline (see Fig. 5 [450, BL-UR]) of a memory device (Fig. 5 [T_M, C_M]).

Regarding independent claim 4, Busch et al. show a sense amplifier circuit (Fig. 4, 5) comprising:

a first sense amplifier (Fig. 4 [405]) having an input coupled to a long bitline (Fig. 4 [450]), a second sense amplifier (Fig. 4 [400]) having an input coupled to a short bitline (Fig. 4 [440]), the input to the second sense amplifier (Fig. 4 [400]) being electrically isolated from the input to the first sense amplifier (Fig. 4 [405]);

an equalizer (Fig. 5 [T7]) connected to the input to the first sense amplifier (Fig. 4 [405]) to provide an equalizing voltage thereto;

an equalizer (Fig. 5 [T3]) connected to the input of the second sense amplifier (Fig. 4 [400]) to provide an equalizing voltage thereto;

and wherein the input to the second sense amplifier (Fig. 4 [400]) may be equalized by the equalizing voltage from the second equalizer (Fig. 5 [T3]) independent from the equalizing voltage from the first equalizer (Fig. 5 [T7]).

Regarding independent claim 6, Busch et al. show an integrated circuit device (Fig. 5), comprising:

a memory array having a plurality of memory cells(see column 5, lines 52-64);

a first signal path (Fig. 5 [450]) that provides access to the plurality of memory cells;

a first sense amplifier (Fig. 5 [405]) connected to the first signal path (Fig. 5 [450]), the first signal path (Fig. 5 [450]) being electrically isolated from a second signal path (Fig. 5 [440]);

and an equalizer (Fig. 5 [T7]) connected to the first signal (Fig. 5 [450]) path to provide an equalizing voltage to the first signal path (Fig. 5 [450]), wherein the first signal path (Fig. 5 [450]) may be equalized by the equalizing voltage independent from a voltage on the second signal path (Fig. 5 [440]).

Regarding dependent claim 8, Busch et al. show the first signal path (Fig. 5 [450]) comprises a bitline (see Fig. 5 [450, BL-UR]).

Regarding dependent claim 9, Busch et al. show an equalizer (Fig. 5 [T3]) coupled to the second signal path (Fig. 5 [440]) to provide an equalizing voltage to the second signal path (Fig. 5 [440]).

8. **Claims 1, 3-4, 6, and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hidaka (U.S. Patent 5,973,983).**

Regarding independent claim 1, Hidaka shows an equalization circuit (Fig. 1) comprising:

a first sense amplifier (Fig. 1 [SAa]) having an input (Fig. 1 [MBLa0]), the input (Fig. 1 [MBLa0]) being electrically isolated from an input (Fig. 1 [MBLa1]) to a second sense amplifier (Fig. 1 [SAb]);

an equalizer (Fig. 1 [EQa]) connected to the input (Fig. 1 [MBLa0]) to the first sense amplifier (Fig. 1 [SAa]) to provide an equalizing voltage to the input (Fig. 1 [MBLa0]) to the first sense amplifier (Fig. 1 [SAa]);

and wherein the input (Fig. 1 [MBLa0]) to the first sense amplifier (Fig. 1 [SAa]) may be equalized by the equalizing voltage independent from the input (Fig. 1 [MBLa1]) to the second sense amplifier (Fig. 1 [SAb]).

Regarding dependent claim 3, Hidaka shows the input (Fig. 1 [MBLa0]) to the first sense amplifier (Fig. 1 [SAa]) comprises a bitline (see Fig. 1 [MBLa0]) of a memory device (Fig. 1 [MCa, MCb]).

Regarding independent claim 4, Hidaka shows a sense amplifier circuit (Fig. 1) comprising:

a first sense amplifier (Fig. 1 [SAa]) having an input (Fig. 1 [MBLa0]) coupled to a long bitline (Fig. 1, 22A [SBLa1]), a second sense amplifier (Fig. 1 [SAb]) having an input (Fig. 1 [MBLa1]) coupled to a short bitline (Fig. 1, 22A [SBLa3]), the input (Fig. 1 [MBLa1]) to the second sense amplifier (Fig. 1 [SAb]) being electrically isolated from the input (Fig. 1 [MBLa0]) to the first sense amplifier (Fig. 1 [SAa]);

an equalizer (Fig. 1 [EQa]) connected to the input (Fig. 1 [MBLa0]) to the first sense amplifier (Fig. 1 [SAa]) to provide an equalizing voltage thereto;

an equalizer connected to the input (Fig. 1 [MBLa1]) of the second sense amplifier (Fig. 1 [SAb]) to provide an equalizing voltage thereto;

and wherein the input (Fig. 1 [MBLa1]) to the second sense amplifier (Fig. 1 [SAb]) may be equalized by the equalizing voltage from the second equalizer (Fig. 1 [EQb]) independent from the equalizing voltage from the first equalizer (Fig. 1 [EQa]).

Regarding independent claim 6, Hidaka shows an integrated circuit device (Fig. 1), comprising:

a memory array (Fig. 1 [B#0-B#3]) having a plurality of memory cells;

a first signal path (Fig. 1 [MBLa0]) that provides access to the plurality of memory cells;

a first sense amplifier (Fig. 1 [SAa]) connected to the first signal path (Fig. 1 [MBLa0]), the first signal path (Fig. 1 [MBLa0]) being electrically isolated from a second signal path (Fig. 1 [MBLa1]);

and an equalizer (Fig. 1 [EQa]) connected to the first signal path (Fig. 1 [MBLa0]) to provide an equalizing voltage to the first signal path (Fig. 1 [MBLa0]), wherein the first signal path (Fig. 1 [MBLa0]) may be equalized by the equalizing voltage independent from a voltage on the second signal path (Fig. 1 [MBLa1]).

Regarding dependent claim 8, Hidaka shows the first signal (Fig. 1 [MBLa0]) path comprises a bitline (see Fig. 1 [MBLa0]).

Regarding dependent claim 9, Hidaka shows an equalizer (Fig. 1 [EQb]) coupled to the second signal path (Fig. 1 [MBLa1]) to provide an equalizing voltage to the second signal path (Fig. 1 [MBLa1]).

9. **Claims 1, 3, 6, and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto (U.S. Patent 5,910,926).**

Regarding independent claim 1, Hashimoto shows an equalization circuit (Fig. 5) comprising:

a first sense amplifier (Fig. 5 [51 in 32A]) having an input (unlabeled bitline Fig. 5 [line connecting 51 in 32A to 55]) the input (unlabeled bitline) being electrically isolated from an input (unlabeled bitline Fig. 5 [line connecting 51 in 32B to 55]) to a second sense amplifier (Fig. 5 [32B]);

an equalizer (Fig. 5 [53 in 32A]) connected to the input to the first sense amplifier (Fig. 5 [51 in 32A]) to provide an equalizing voltage to the input to the first sense amplifier (Fig. 5 [51 in 32A]);

and wherein the input to the first sense amplifier (Fig. 5 [51 in 32A]) may be equalized by the equalizing voltage independent from the input to the second sense amplifier (Fig. 5 [51 in 32B]).

Regarding dependent claim 3, Hashimoto shows the input to the first sense amplifier (Fig. 5 [51 in 32A]) comprises a bitline of a memory device (Fig. 5 [55]).

Regarding independent claim 6, Hashimoto shows an integrated circuit device (Fig. 5), comprising:

a memory array (Fig. 5 [31]) having a plurality of memory cells;

a first signal path (unlabeled bitline Fig. 5 [line connecting 51 in 32A to 55]) that provides access to the plurality of memory cells;

a first sense amplifier (Fig. 5 [51 in 32A]) connected to the first signal path, the first signal path being electrically isolated from a second signal path (unlabeled bitline Fig. 5 [line connecting 51 in 32B to 55]);

and an equalizer (Fig. 5 [53 in 32A]) connected to the first signal path to provide an equalizing voltage to the first signal path, wherein the first signal path may be equalized by the equalizing voltage independent from a voltage on the second signal path.

Regarding dependent claim 8, Hashimoto shows the first signal path comprises a bitline (see unlabeled bitline Fig. 5 [line connecting 51 in 32A to 55]).

Regarding dependent claim 9, Hashimoto shows an equalizer (Fig. 5 [53 in 32B]) coupled to the second signal path to provide an equalizing voltage to the second signal path.

10. **Claims 1, 3, 6, and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Min et al. (U.S. Patent 5,402,378).**

Regarding independent claim 1, Min et al. show an equalization circuit comprising (Fig. 1):

a first sense amplifier (Fig. 1 [3]) having an input (Fig. 1 [BL1]), the input being electrically isolated from an input (Fig. 1 [BL2]) to a second sense amplifier (Fig. 1 [6]);

an equalizer (Fig. 1 [2]) connected to the input (Fig. 1 [BL1]) to the first sense amplifier (Fig. 1 [3]) to provide an equalizing voltage to the input (Fig. 1 [BL1]) to the first sense amplifier (Fig. 1 [3]);

and wherein the input (Fig. 1 [BL1]) to the first sense amplifier (Fig. 1 [3]) may be equalized by the equalizing voltage independent from the input (Fig. 1 [BL2]) to the second sense amplifier (Fig. 1 [6]).

Regarding dependent claim 3, Min et al. show the input (Fig. 1 [BL1]) to the first sense amplifier (Fig. 1 [3]) comprises a bitline (Fig. 1 [BL1]) of a memory device (Fig. 1 [1]).

Regarding independent claim 6, Min et al. show an integrated circuit device (Fig. 1), comprising:

a memory array (Fig. 1 [1]) having a plurality of memory cells;

a first signal path (Fig. 1 [BL1]) that provides access to the plurality of memory cells;

a first sense amplifier (Fig. 1 [3]) connected to the first signal path (Fig. 1 [BL1]), the first signal path (Fig. 1 [BL1]) being electrically isolated from a second signal path (Fig. 1 [BL2]);

and an equalizer (Fig. 1 [2]) connected to the first signal path (Fig. 1 [BL1]) to provide an equalizing voltage to the first signal path (Fig. 1 [BL1]), wherein the first signal path (Fig. 1 [BL1]) may be equalized by the equalizing voltage independent from a voltage on the second signal path (Fig. 1 [BL2]).

Regarding dependent claim 8, Min et al. show the first signal path (Fig. 1 [BL1]) comprises a bitline (Fig. 1 [BL1]).

Regarding dependent claim 9, Min et al. show an equalizer (Fig. 1 [7]) coupled to the second signal path (Fig. 1 [BL2]) to provide an equalizing voltage to the second signal path (Fig. 1 [BL2]).

11. **Claims 1, 3, 6, and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujino (U.S. Patent Application Publication 2002/0141228).**

Regarding independent claim 1, Fujino shows an equalization circuit (Fig. 6) comprising:

a first sense amplifier (Fig. 6 [3L]) having an input (Fig. 6 [BLL1]), the input (Fig. 6 [BLL1]) being electrically isolated from an input (Fig. 6 [BLL0]) to a second sense amplifier (Fig. 6 [3R]);

an equalizer (Fig. 6 [6La]) connected to the input (Fig. 6 [BLL1]) to the first sense amplifier (Fig. 6 [3L]) to provide an equalizing voltage to the input (Fig. 6 [BLL1]) to the first sense amplifier (Fig. 6 [3L]);

and wherein the input (Fig. 6 [BLL1]) to the first sense amplifier (Fig. 6 [3L]) may be equalized by the equalizing voltage independent from the input (Fig. 6 [BLL0]) to the second sense amplifier (Fig. 6 [3R]).

Regarding dependent claim 3, Fujino shows the input to the first sense amplifier (Fig. 6 [3L]) comprises a bitline (Fig. 6 [BLL1]) of a memory device (Fig. 6 [MC]).

Regarding independent claim 6, Fujino shows an integrated circuit device (Fig. 6), comprising:

a memory array (Fig. 6 [MAb]) having a plurality of memory cells;

a first signal path (Fig. 6 [BLL1]) that provides access to the plurality of memory cells;

a first sense amplifier (Fig. 6 [3L]) connected to the first signal path (Fig. 6 [BLL1]), the first signal path (Fig. 6 [BLL1]) being electrically isolated from a second signal path (Fig. 6 [BLL0]);

and an equalizer (Fig. 6 [6La]) connected to the first signal path (Fig. 6 [BLL1]) to provide an equalizing voltage to the first signal path (Fig. 6 [BLL1]), wherein the first signal path (Fig. 6 [BLL1]) may be equalized by the equalizing voltage independent from a voltage on the second signal path (Fig. 6 [BLL0]).

Regarding dependent claim 8, Fujino shows the first signal path (Fig. 6 [BLL1]) comprises a bitline (Fig. 6 [BLL1]).

Regarding dependent claim 9, Fujino shows an equalizer (Fig. 6 [6Ra]) coupled to the second signal path (Fig. 6 [BLL0]) to provide an equalizing voltage to the second signal path (Fig. 6 [BLL0]).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 10, and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Busch et al. (U.S. Patent 4807195) in view of Bashir (U.S. Patent 5,594,691).**

Regarding independent claim 10, Busch et al. teach all of the limitations from claim 6 (which are included in independent claim 10; see Busch et al. rejection of claim 6). Busch et al. are silent with respect to: a processor adapted to execute instructions; a storage device adapted to store instructions to be executed by the processor; and a memory device that specifically receives information stored on the storage device.

Bashir shows a generic block diagram of a computer system including a processor (Bashir Fig 1 [12]), a storage device (Bashir Fig 1 [17]), and memory device (Bashir Fig 1 [16]) that receives information stored on the storage device (Fig. 1 [17]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Busch et al. such that the memory of Busch et al. replaces the SRAM of Bashir for the purpose of implementing the memory of Busch et al. into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Busch et al. are commonly classified in class 365 (Static memories).

Regarding dependent claim 12, Busch et al. show the first signal path (Fig. 5 [450]) comprises a bitline (see Fig. 5 [450, BL-UR]).

Regarding dependent claim 13, Busch et al. show an equalizer (Fig. 5 [T3]) coupled to the second signal path (Fig. 5 [440]) to provide an equalizing voltage to the second signal path (Fig. 5 [440]).

Regarding dependent claim 14, Busch et al. in view of Bashir teach all of the limitations as discussed above. Busch et al. are silent with respect to a user input device adapted to receive data for use by the processor.

Bashir shows a generic block diagram of a computer system including a keyboard (Bashir Fig 1 [22]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Busch et al. such that the memory of Busch et al. replaces the SRAM of Bashir for the purpose of implementing the memory of Busch et al. into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Busch et al. are commonly classified in class 365 (Static memories).

Regarding dependent claim 15, Busch et al. in view of Bashir teach all of the limitations as discussed above. Busch et al. are silent with respect to a display device adapted to produce an image for viewing by a user based on instructions executed by the processor.

Bashir shows a generic block diagram of a computer system including a display device (Bashir Fig 1 [21]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Busch et al. such that the memory of Busch et al. replaces the SRAM of Bashir for the purpose of implementing the memory of Busch et al. into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Busch et al. are commonly classified in class 365 (Static memories).

14. **Claims 10, and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka (U.S. Patent 5,973,983) in view of Bashir (U.S. Patent 5,594,691).**

Regarding independent claim 10, Hidaka teaches all of the limitations from claim 6 (which are included in independent claim 10; see Hidaka rejection of claim 6). Hidaka is silent with respect to: a processor adapted to execute instructions; a storage device adapted to store instructions to be executed by the processor; and a memory device that specifically receives information stored on the storage device.

Bashir shows a generic block diagram of a computer system including a processor (Bashir Fig 1 [12]), a storage device (Bashir Fig 1 [17]), and memory device (Bashir Fig 1 [16]) that receives information stored on the storage device (Fig. 1 [17]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Hidaka such that the memory of Hidaka replaces the SRAM of Bashir for the purpose of implementing the memory of Hidaka into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Hidaka are commonly classified in class 365 (Static memories).

Regarding dependent claim 12, Hidaka shows the first signal (Fig. 1 [MBLa0]) path comprises a bitline (see Fig. 1 [MBLa0]).

Regarding dependent claim 13, Hidaka shows an equalizer (Fig. 1 [EQb]) coupled to the second signal path (Fig. 1 [MBLa1]) to provide an equalizing voltage to the second signal path (Fig. 1 [MBLa1]).

Regarding dependent claim 14, Hidaka in view of Bashir teach all of the limitations as discussed above. Hidaka is silent with respect to a user input device adapted to receive data for use by the processor.

Bashir shows a generic block diagram of a computer system including a keyboard (Bashir Fig 1 [22]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Hidaka such that the memory of Hidaka replaces the SRAM of Bashir for the purpose of implementing the memory of Hidaka into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Hidaka are commonly classified in class 365 (Static memories).

Regarding dependent claim 15, Hidaka in view of Bashir teach all of the limitations as discussed above. Hidaka is silent with respect to a display device adapted to produce an image for viewing by a user based on instructions executed by the processor.

Bashir shows a generic block diagram of a computer system including a display device (Bashir Fig 1 [21]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Hidaka such that the memory of Hidaka replaces the SRAM of Bashir for the purpose of implementing the memory of Hidaka into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Hidaka are commonly classified in class 365 (Static memories).

15. **Claims 10, and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (U.S. Patent 5,910,926) in view of Bashir (U.S. Patent 5,594,691).**

Regarding independent claim 10, Hashimoto teaches all of the limitations from claim 6 (which are included in independent claim 10; see Hashimoto rejection of claim 6). Hashimoto further teaches a central processing unit (processor; see column 1, line 21). Hashimoto is silent with respect to: a storage device adapted to store instructions to be executed by the processor; and a memory device that specifically receives information stored on the storage device.

Bashir shows a generic block diagram of a computer system including a storage device (Bashir Fig 1 [17]), and memory device (Bashir Fig 1 [16]) that receives information stored on the storage device (Fig. 1 [17]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Hashimoto such that the memory of Hashimoto replaces the SRAM of Bashir for the purpose of implementing the memory of Hashimoto into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Hashimoto are commonly classified in class 365 (Static memories).

Regarding dependent claim 12, Hashimoto shows the first signal path comprises a bitline (see unlabeled bitline Fig. 5 [line connecting 51 in 32A to 55]).

Regarding dependent claim 13, Hashimoto shows an equalizer (Fig. 5 [53 in 32B]) coupled to the second signal path to provide an equalizing voltage to the second signal path.

Regarding dependent claim 14, Hashimoto in view of Bashir teach all of the limitations as discussed above. Hashimoto is silent with respect to a user input device adapted to receive data for use by the processor.

Bashir shows a generic block diagram of a computer system including a keyboard (Bashir Fig 1 [22]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Hashimoto such that the memory of Hashimoto replaces the SRAM of Bashir for the purpose of implementing the memory of Hashimoto into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Hashimoto are commonly classified in class 365 (Static memories).

Regarding dependent claim 15, Hashimoto in view of Bashir teach all of the limitations as discussed above. Hashimoto is silent with respect to a display device adapted to produce an image for viewing by a user based on instructions executed by the processor.

Bashir shows a generic block diagram of a computer system including a display device (Bashir Fig 1 [21]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Hashimoto such that the memory of Hashimoto replaces the SRAM of Bashir for the purpose of implementing the memory of Hashimoto into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Hashimoto are commonly classified in class 365 (Static memories).

16. **Claims 10, and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Min et al. (U.S. Patent 5,402,378) in view of Bashir (U.S. Patent 5,594,691).**

Regarding independent claim 10, Min et al. teach all of the limitations from claim 6 (which are included in independent claim 10; see Min et al. rejection of claim 6). Min et al. are silent with respect to: a processor adapted to execute instructions; a storage device adapted to store instructions to be executed by the processor; and a memory device that specifically receives information stored on the storage device.

Bashir shows a generic block diagram of a computer system including a processor (Bashir Fig 1 [12]), a storage device (Bashir Fig 1 [17]), and memory device (Bashir Fig 1 [16]) that receives information stored on the storage device (Fig. 1 [17]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Min et al. such that the memory of Min et al. replaces the SRAM of Bashir for the purpose of implementing the memory of Min et al. into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Min et al. are commonly classified in class 365 (Static memories).

Regarding dependent claim 12, Min et al. show the first signal path (Fig. 1 [BL1]) comprises a bitline (Fig. 1 [BL1]).

Regarding dependent claim 13, Min et al. show an equalizer (Fig. 1 [7]) coupled to the second signal path (Fig. 1 [BL2]) to provide an equalizing voltage to the second signal path (Fig. 1 [BL2]).

Regarding dependent claim 14, Min et al. in view of Bashir teach all of the limitations as discussed above. Min et al. are silent with respect to a user input device adapted to receive data for use by the processor.

Bashir shows a generic block diagram of a computer system including a keyboard (Bashir Fig 1 [22]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Min et al. such that the memory of Min et al. replaces the SRAM of Bashir for the purpose of implementing the memory of Min et al. into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Min et al. are commonly classified in class 365 (Static memories).

Regarding dependent claim 15, Min et al. in view of Bashir teach all of the limitations as discussed above. Min et al. are silent with respect to a display device adapted to produce an image for viewing by a user based on instructions executed by the processor.

Bashir shows a generic block diagram of a computer system including a display device (Bashir Fig 1 [21]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Min et al. such that the memory of Min et al. replaces the SRAM of Bashir for the purpose of implementing the memory of Min et al. into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Min et al. are commonly classified in class 365 (Static memories).

17. **Claims 10, and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujino (U.S. Patent Application Publication 2002/0141228) in view of Bashir (U.S. Patent 5,594,691).**

Regarding independent claim 10, Fujino teaches all of the limitations from claim 6 (which are included in independent claim 10; see Fujino rejection of claim 6). Fujino further teaches a portable information terminal, or communication terminal for the Internet to deal with large amounts of image data and audio data (paragraph 0004). However, Fujino is explicitly silent with respect to a processor adapted to execute instructions; a storage device adapted to store instructions to be executed by the processor; and a memory device that specifically receives information stored on the storage device.

Bashir shows a generic block diagram of a computer system including a processor (Bashir Fig 1 [12]), a storage device (Bashir Fig 1 [17]), and memory device (Bashir Fig 1 [16]) that receives information stored on the storage device (Fig. 1 [17]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Fujino such that the memory of Fujino replaces the SRAM of Bashir for the purpose of implementing the memory of Fujino into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Fujino are commonly classified in class 365 (Static memories).

Regarding dependent claim 12, Fujino shows the first signal path (Fig. 6 [BLL1]) comprises a bitline (Fig. 6 [BLL1]).

Regarding dependent claim 13, Fujino shows an equalizer (Fig. 6 [6Ra]) coupled to the second signal path (Fig. 6 [BLL0]) to provide an equalizing voltage to the second signal path (Fig. 6 [BLL0]).

Regarding dependent claim 14, Fujino in view of Bashir cover all of the limitations as discussed above. Fujino is silent with respect to a user input device adapted to receive data for use by the processor.

Bashir shows a generic block diagram of a computer system including a keyboard (Bashir Fig 1 [22]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Fujino such that the memory of Fujino replaces the SRAM of Bashir for the purpose of implementing the memory of Fujino into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Fujino are commonly classified in class 365 (Static memories).

Regarding dependent claim 15, Fujino in view of Bashir cover all of the limitations as discussed above. Fujino is silent with respect to a display device adapted to produce an image for viewing by a user based on instructions executed by the processor.

Bashir shows a generic block diagram of a computer system including a display device (Bashir Fig 1 [21]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Bashir to the teachings of Fujino such that the memory of Fujino replaces the SRAM of Bashir for the purpose of implementing the memory of Fujino into a computer system. Further motivation to perform the above stated modification is evidented by the fact that memories are used in computer systems and that both Bashir and Fujino are commonly classified in class 365 (Static memories).

Allowable Subject Matter

18. **Claims 2, 5, 7, and 11 are objected to as being dependent upon a rejected base claim**, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is a statement of reasons for the indication of allowable subject matter:

With respect to dependent claims 2, and 5, there is no teaching or suggestion in the prior art to electrically isolating the sense amplifiers by means of a capacitor.

With respect to dependent claims 7, and 11, there is no teaching or suggestion in the prior art to electrically isolating a first sense amplifier (connected to a first bit line) from a second signal path (a second bitline) by means of a capacitor.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Faue et al. (U.S. Patent Application Publication 2006/0023529)

Faue et al. show a circuit with data line pairs, sense amplifiers, equalizers, and memory arrays to quickly and efficiently equalizing data line pairs so that the adverse affects of distributed resistance and capacitance in long data lines can be overcome. This reference was filed after instant application.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

Tuan T. Nguyen
3/4/06